TIMING PERFORMANCE ANALYSIS

ABSTRACT

Method to determine path timing to and from an embedded device is described. More particularly, clock-to-output delays, interconnects and interconnect logic delays, and setup and hold times for input and output paths from a microprocessor core and a memory controller are obtained and determined, as applicable. These times are assembled in a spreadsheet for associating with respective signals. Times for each of the signals are totaled to determine respective path delays for comparison with a target clock period.